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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

02530022cc

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Signature _____

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name _____

Application Number

09/837,190

Filed

4/19/01

First Named Inventor

Sawada

Art Unit

2616

Examiner

Vent

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

☐

applicant/inventor.

☐

assignee of record of the entire interest.

See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒

attorney or agent of record.

Registration number 32,635

☐

attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34 _____

Signature

Michael Whitham

Typed or printed name

703-787-9400

Telephone number

March 20, 2001

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐

*Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Hideki Sawada

Confirmation No. 1193

Serial No. 09/837,190

Group Art Unit: No. 2616

Filed April 19, 2001

Examiner Jamie J. Vent

For RECORDING/REPRODUCING SYSTEM

Mail Stop AF

Commissioner for Patents

PO Box 1450

Alexandria, Virginia 22313-1450

ATTACHMENT TO PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

This Pre-Appeal Brief Request for Review is being concurrently filed with a Notice of Appeal. A check is attached to satisfy the fees for the Notice of Appeal. If any additional fees are required to satisfy the fees due for the Notice of Appeal or to gain entry and consideration of this Pre-Appeal Brief Request for Review, the Commissioner is authorized to charge Attorney's Deposit Account 50-2041 (Whitham, Curtis & Christofferson).

The Invention

The invention is directed to real time recording/reproducing systems for recording and real time (instantaneously) reproducing image (or video) data. The invention solves a specific problem of such systems that make use of personal computer (PC) software processing. Performance insufficiency of the CPU may arise when the system is operated in parallel with other applications or at the moment of starting the same. In consequence, it becomes impossible to obtain full frame real time capturing, real time compression and real time decompression. This leads to missing of frame data in the compression processing and delay in the reproducing processing and also to a further problem of deviation from

synchronism of image and voice to each other.

As shown in Figure 1, an ADC 102 receives an analog image signal from an image input terminal 101. The output from the ADC 102 is to a frame memory 103, followed by a compression processing module 104, and then a recorder 105. A digital signal read from the recorder 105 is input to a decompression processing module 106, followed by a frame memory 107 and a DAC 108, so that a reproduced video signal is output at output terminal 109. A frame rate controller 110 executes a frame interpolation process such as to provide a constant frame rate of reading of data from the frame memory 103 to the compression processing module 104. The compression processing module 104 executes digital compression processing in a compressing system, which conforms to, for instance, MPEG standards. The compression and decompression processing modules 104 and 106 constitute CPU software processing parts, the ADC 102 may be a video capture card, the frame memories 103 and 107 may be, for example, memories such as main memory and video memory, the DAC 108 may be a graphic accelerator card, and the recorder 105 may be constituted by a hard disc drive or the like.

When the system becomes unable to execute full frame real time processing due to the CPU performance insufficiency, the frame rate controller 110 executes a control process of controlling the frame rate of data read out from the frame memory 103 to the compression processing module 104 to be constant. When the compression processing module 104 becomes unable to execute full frame real time compression processing, it executes a thinning-out process, in which compression processing on some frames is omitted, thus generating digital compressed data at a substantially reduced frame rate while retaining a fixed standard frame rate. The decompression processing module 106 has a frame skipping function of skipping some frames in the decompression processing for reproduction synchronous to voice data with omitting a part of the frame decompression process. The frame rate controller 110 holds a constant intrinsic frame rate at all times by executing the frame interpolating processing in the event when the system becomes unable to execute full frame real time frame capturing.

The manner in which this is done is described in detail at pages 10–18 of the specification with reference to Figures 2–9.

Errors and Omissions

The Examiner has failed to make out a *prima facie* case of obviousness under 35 U.S.C. §103 but has, instead, relied on hindsight in an attempt to piece together several disparate references to arrive at his conclusion of obviousness. Specifically, the Examiner rejects claims 1 and 9–12 as being unpatentable over Takahashi et al. (US 5,966,495) in view of Tanaka et al. (US 6,163,646) and Honda et al. (US 6,608,938), claims 2, 3, 4, 6, and 7 as unpatentable over Takahashi et al. ('495) in view of Tanaka et al. ('646), Honda et al. ('938) and Honda et al. (US 2004/0240744), and claims 5 and 8 as unpatentable over Takahashi et al. ('495) in view of Tanaka et al. ('646), Honda et al. ('938), Honda et al. ('744), and Fujinami et al. (US 6,697,566).

Takahashi et al. neither recognize nor solve the problem solved by the claimed invention, to wit, performance insufficiency of the CPU when the system is operated in parallel with other applications or at the moment of starting the same and, in consequence, it becomes impossible to obtain full frame real time capturing, real time compression and real time decompression, leading to missing of frame data in the compression processing and delay in the reproducing processing and also to a further problem of deviation from synchronism of image and voice to each other. Tanaka et al. disclose an apparatus for a synchronized playback of compressed digital data of audio-video signals with a simple configuration to be applied to a system having comparatively low data processing ability, independent of resolution of a software timer of the system, the apparatus of the invention obtains a reference time indicating reproduction time passage of the audio signal component from reproduced data amount of the audio signal component, and detects progress of the video signal component in reference to the reference time.

Honda et al. ('938) disclose an image data compression or expansion

method and apparatus for use in a remote monitoring system which employs an image change detection means for detecting a change in image based on input image data and means for controlling a frame rate of outputted compressed image data. In other words, Honda et al. provide a variable frame rate depending on the rate of motion of an input image. This is quite different from what the claimed invention accomplishes. Specifically, the claimed invention aims to control the frame rate of the compression processing module to be constant by executing a frame interpolating processing. Clearly, there is no possibility of modifying the combined teachings of Takahashi et al. and Tanaka et al. with that of Honda et al. and arriving at the claimed invention. Note that Honda et al. ('744) is a continuation of the application on which Honda et al. ('938) issued and therefore has the identical same disclosure.

Fujinami et al. address the problem of recording pre-compressed MPEG files while maintaining management information for indicating sector positions, a process which normally required decoding and re-encoding followed by recording with a consequent loss of video quality. What Fujinami et al. do is to provide a characteristic point detection circuit which detects a characteristic point from a base band video signal and generate a characteristic point file. This characteristic point file is multiplexed with the MPEG compressed video file which is recorded to optical disc and, during reproduction from the video disc, the characteristic point file is used to indicate sector positions for random access.

Conclusion

None of the references relied on by the Examiner show or suggest "a frame rate controller for controlling the compression processing module *to hold a constant intrinsic frame rate by executing frame interpolating processing*", as specifically recited in claim 1, for example. Therefore, no combination of the references can possibly suggest or teach this feature. The reason is simple – none of the references recognize, much less, solve the problem solved by the disclosed and claimed invention, which is real time recording and real time reproducing

image or video data when the system becomes unable to execute full frame real time processing due to the CPU performance insufficiency. The Applicant solves this problem in a unique and elegant manner by providing a frame rate controller that executes a control process of controlling the frame rate of data read out from the frame memory to the compression processing module to be constant, and when the compression processing module becomes unable to execute full frame real time compression processing, it executes a thinning-out process, in which compression processing on some frames is omitted, thus generating digital compressed data at a substantially reduced frame rate while retaining a fixed standard frame rate. Further, the decompression processing module has a frame skipping function of skipping some frames in the decompression processing for reproduction synchronous to voice data with omitting a part of the frame decompression process. The frame rate controller holds a constant intrinsic frame rate at all times by executing the frame interpolating processing in the event when the system becomes unable to execute full frame real time frame capturing. The Examiner's attempted hindsight reconstruction of multiple disparate references does not accomplish this result.

In view of the above, it is requested that the position of the Examiner be reviewed, that the rejections be withdrawn, and that the application be passed to issue.

Respectfully submitted,



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